INTEGRATED PRECISION TUNING SYSTEM

Sixth Quarterly Progress Report

1 December 1962 To 20 February 1963

Report No. 6

CONTRACT NO. DA-36-039-SC-88908

SCTR NO. SCL-7566A (11 JANUARY 1961)

DA NO. 3D26-02-001

405 973

U.S. Army Electronic Research and Development Laboratory,

Fort Monmouth, New Jersey

GENERAL DYNAMICS | ELECTRONICS-ROCHESTER

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1 December 1962 to 28 February 1963

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1. PURPOSE

This is the Sixth Quarterly Report discussing progress in the development of an electronically controlled tuning system. The objective of this task is the development of an electronically controlled tuning system leading to the establishment of a prototype for future electronic communications equipment tuner needs, and the basis for future development and study. The first task of the program is to study, investigate, and develop an accurate method of electronically tuning an RF front end covering the 3 to 12 mc/s range. The detailed system objectives of the tuner are spedified in Signal Corps Technical Requirement SCL-7566A. Other tasks in the program are the development of (a) two experimental models and (b) two developmental models.

2. ABSTRACT

A review of the work performed during the first phase of this program is presented in this report. A description of the design considerations and problem areas leading to the present design is given. Data on the Digital Coarse Tuning Scheme is presented as well as schematics and description of operation. A discussion of voltage variable capacitor characterics required to accomplish octave tuning is also presented.

3. CONFERENCES

3.1 Telephone Conversation with USAERDL, Ft. Monmouth, New Jersey on 2 January 1963

The possibility of a late delivery of the Development Models of the Precision Tuner was brought to the attention of R. Tilton of USAERDL. Difficulty with obtaining from a vendor the wafer switches used for band switching was discussed, and it was decided that a two week delivery extension should be sought, since General Dynamics/Electronics would have to make the wafers in-house. A request for the extension was to be initiated by G. Luhowy of GD/E.

3.2 Telephone Conversation with USAERDL, Ft. Monmouth, New Jersey on 24 January 1963

Mr. R. Tilton of USAERDL was informed of the difficulty of plating through the holes in the wafer switches. The first set of wafers was not usable because the plating did not adhere in the holes and a new set must be made. A request for extension of delivery to 28 February 1963 was to be initiated in order to fabricate and test a new set of wafers.

3.3 Conference with USAERDL at General Dynamics/Electronics, Rochester, New York on January 30 and 31, 1963

The Fifth Quarterly Report was discussed, and a number of points were made as follows:

a. Report No. 5 did not state which coarse tuning scheme was chosen for the Development Models. This was to be covered in Report No. 6.

b. Final data on AGC, phase locked loop, battery drain etc., for the Development Models should be included in Report No. 6.

c. A complete rundown of the Technical Specification would be made in testing the Development Models except for temperature and humidity. Regarding temperature testing, a discussion of a modification to the present design consisting essentially of replacing the present coils with temperature-stable ones was held. This

discussion would be presented (along with other recommendations) in the test data to be forwarded with the Development Models.

d. The life test specification was discussed with regard to digital tuning. Since the specification was written for a continuously tunable element, such as a potentiometer or variable capacitor, it was agreed that it did not apply directly to this design. Therefore, the following data would be supplied:

1. Life test data for the wafers used for band switching.
2. Applicable Military specifications for the digital frequency selector switches. No life test of the Geneva mechanism which accomplishes RF band switching would be required.

3.4 Telephone Conversation with Amperex Corporation, Hicksville, Long Island, New York on 8 February 1963

Mr. Edward King of Amperex called to obtain information about the requirements for a voltage variable capacitor which would accomplish the tuning of the Precision Integrated Tuner. He was given the tentative specification for a 150/250 pf at 8V back to back diode or 300/500 pf at 8V single diode with a Q = 250 at 8V at 16 mc. This tentative specification was generated during the last phases of the present design and has been used as a preliminary goal in discussions concerning requirements for a VVC diode for this program. (See paragraph 4.2 of this report.)

3.5 Telephone Conversation with USAERDL, Ft. Monmouth, New Jersey on 13 February 1963

Mr. Tilton was called to be informed on the status of the wafer switches. A problem developed with the switches due to our plating technique. Life test data had shown that considerable improvement in contact wear could be obtained by plating the wafer sections with nickel followed by a rhodium flash. However, because the chemically deposited copper which plates the feed-through holes in the wafer switches does not have a very high bond strength, platings applied on top of this layer peeled off, particularly the nickel which is quite inflexible. To

eliminate this peeling, it was found necessary to strip all the chemically deposited copper from the switch contact surfaces and plate directly on the laminated copper. This involved reworking all of the wafer boards, and resulted in a slippage in the fabrication schedule. To minimize the time lost, it was agreed that the boards would be gold plated over the laminate copper rather than risk a faulty nickel plate, since nickel plating is considerably more difficult than gold plating. The contact life was expected to be lessened, but if life test data was satisfactory, no objection would be raised.

3.6 Conference with Philco Corp., Lansdale, Pennsylvania at General Dynamics/Electronics, Rochester, New York on 15 February 1963

A conference was held with Mr. Charles R. Gray of Philco Corp. to discuss further the high-Q Philco Voltacap ®. A most informative discussion took place during which Mr. Gray described the technology required to make a high-Q high capacitance voltage variable capacitor. (No attempt to describe this technology will be made here. Interested parties should contact Mr. Gray directly.)

Pertinent to this program was the indication that the initial capacitance at 8V bias could be held to ±20 per cent with ease, ±10 per cent less easily, but ±5 per cent should be looked upon as a goal. Selected tolerance units would be available, of course, but the yield would be low and the cost correspondingly high. It was expected that 250 pf and 500 pf devices would be in preproduction in the second half of 1963 with production beginning the end of 1963.

Mr. Gray furnished selected samples of some new devices with the following characteristics (typical)

C 8V = 500 pf ±20 per cent

Q at 8V at 10 mc = 325 ±25

Q at 8V at 16 mc (estimated) = 210

C 4.5/C 150V = 5.1

V_R | 25 μa ≅ 160V

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While this device does not yet have a 200 volt back voltage, such a characteristic is theoretically possible, and a few such diodes have been made. Refinements in the control of the manufacturing process will probably lead to the ability to reproduce such devices. Philco is presently working toward such a goal.

3.7 Conference with Pacific Semiconductor Inc. at General Dynamics/ Electronics, Rochester, New York on 19 February 1963

Messrs. Henry W. DeMond and Cal Taintor of PSI met with F. S. J. Daniel and G. J. Luhowy of GD/E to discuss a 500 pf voltage variable capacitor. Mr. DeMond told of PSI's intended extension of its VVC product line. A number of development devices were discussed, and indications are that the tentative specification which has been drawn up by General Dynamics/Electronics is feasible. He pointed out, however, that a definite gap exists between the theoretical and practical limits, particularly if production units are desired. Specific information on PSI devices would be sent to GD/E in the near future.

4. FACTUAL DATA

4.1 Review of the Program to Date - General

A chronological review of the progress and experimentation will be undertaken in this section in order to more clearly define the present design capabilities, deficiencies, and expected future improvements.

4.1.1 Crossmodulation Distortion Caused by the Voltage Variable Capacitor (Report No. 1)

During the initial phases of this program, time was devoted to the study of crossmodulation generated by the voltage variable capacitors (VVC) used in single and double tuned circuits. In Report No. 1 it was determined empirically that the least crossmodulation occurred when VVC's were used in a series back to back configuration, and that the crossmodulation could be minimized by keeping the DC bias voltage high compared to the AC undesired signal. In a double tuned circuit configuration, it was shown that most of the crossmodulation came from the input tuned circuit, and that by replacing the VVC with a fixed mica capacitor, the specification limit could be met. With the VVC in the first tuned circuit, the slope of the crossmodulation response was shown to be -6 db/octave while the overall selectivity of the double tuned circuit was -12 db/octave on the skirts. This also indicated that the distortion is generated mostly in the input circuit since the attenuation characteristic of a single tuned circuit is -6 db/octave. Using a greater number of VVC's per tuned circuit tended to reduce the crossmodulation generated but a compromise had to be made because the improvement per back to back pair diminished while the volume required to package the devices increased. A limit of three back to back pairs (6 VVC's) per tuned circuit was considered reasonable.

It was initially felt that the crossmodulation caused by the VVC's would be independent of the tuned circuit Q's, but this has subsequently been modified. Work continued on the optimumizing of the double tuned circuit and this was reported at the end of the Third Quarter.

The minimum VVC bias was set at 9 volts. Crossmodulation was severe at this voltage, but to set a higher minimum voltage would further reduce an already small available capacitance ratio, and hence, the tuning ratio per band would be reduced requiring a larger number of bands to cover the frequency range.

4.1.2 Tuning and Tracking Considerations

4.1.2.1 Selecting the Bands (Report No. 1)

Choosing a bias voltage range of 9 to 70 volts for the PSI PC-114 Varicap ® (which has been used throughout for the VVC), a capacitance ratio of 2.5:1 is available. Circuit stray and trim capacitance reduces the final available ratio, however, and it was shown that a minimum of four bands would be required to tune the 3 to 12 mc range. It would have been most desirable from a tuning voltage viewpoint to make all bands have the same ratio, because the tracking voltage problem would be simplified as will be explained later. However, since digital tuning was a design requirement, considerable mechanical complexity in the final equipment would be eliminated, if the bands began and ended on even mc increments. It is impossible to break the 3 to 12 mc frequency range into four bands of equal tuning ratio and still begin and end on even mc increments, however, so a method of accurately tracking bands of different tuning ratios had to be developed. Furthermore, four bands beginning and ending on even mc increments such as: (1) 3-4 mc/s, (2) 4-6 mc/s, (3) 6-8 mc/s, and (4) 8-12 mc/s resulted in bands (2) and (4) requiring a 2.25:1 capacitance ratio to tune. With six PC-114 Varicaps in a series back to back configuration, the allowable stray capacitance would be only 4 pf. Since it was estimated that a minimum of 10 pf stray capacitance could be expected, a different solution was required, and we chose to go to five bands, 3-4 mc, 4-5 mc, 5-7 mc, 7-9 mc and 9-12 mc. In this arrangement band 3 is the worst case, having 12 pf allowable stray.

4.1.2.2 The Tracking Requirement (Report No. 2)

In Report No. 2 it was shown that for an RF amplifier

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to be used with a frequency synthesizer the allowable tracking error is related to the loaded tuned circuit Q's. These, in turn, are determined by system objectives such as crossmodulation, image and IF rejection and so on, and having been chosen to meet a tracking specification, such as 1 db per tuned circuit, the allowable mistuning is given by the 1 db bandwidth of a tuned circuit of that loaded Q. Thus as an example, a single tuned circuit of loaded Q = 75 can be mistuned by approximately 18 kc.

Sources of tracking error were investigated. These included errors generated in a bias network designed to generate the required voltage versus frequency characteristic to obtain "straight line" digital tuning. Using five bands to cover the 3 to 12 mc frequency range, four different tuning ratios are required. This means that four different non-linear frequency versus voltage laws are necessary, and it is shown that if an average curve is chosen, finite tuning errors result on all bands. The magnitude of these errors make up an appreciable portion of the 1 db bandwidth of the RF tuned circuits.

In addition, errors result from the component tolerances on the tuned circuit inductance and the VVC's with a 455 kc IF, the tracking error between the local oscillator and the signal circuits is shown to be negligibly small.

4.1.2.3 Automatic Tracking Configurations (Report No. 2)

Since the tracking error between the signal and oscillator circuits was shown to be negligibly small if the oscillator circuit is properly designed, and since both oscillator and signal circuits are tuned in the same manner, i.e., by VVC/s, if the oscillator were locked to an external frequency standard, the voltage which tuned the oscillator VVC/s could be used to tune the signal circuit VVC/s, thereby, eliminating the accumulation of tuning errors. This portion of a patent application of Mr. J. E. Harrison of General Dynamics/Electronics which applies to this program was investigated in detail. Essential to the proper operation of such a technique is that the capacitance versus voltage law of the VVC's be quite close, and that the tuned circuit

inductances be fairly accurate, but errors generated in synthesizing the voltage to tune the circuitry are cancelled out.

Report No. 2 then discussed in detail methods of approach to the problem of locking the VVC controlled local oscillator to an external frequency synthesizer. Basically, the oscillator was placed in a phase-locked loop and since the maximum output voltage from a phase-locked loop is limited to, say ±10 volts, two voltages were applied to the VVC's in order to obtain the 9 to 70 volt range required to tune each band of frequency. A coarse tuning voltage was generated in digital increments such that when applied to both signal and oscillator VVC/s, the oscillator was tuned to within the capture range of the phase detector, (the synthesizer assumed to be at the desired lock frequency) whereupon the phase-locked loop added or subtracted voltage on the VVC's correcting the oscillator frequency and thereby providing a fine tuning control. A discussion of loop stability, capture range, holding range, and other design criteria was given in Report No. 2.

4.1.3 Design of the RF Amplifier Stages - General

Having established that the VVC's were going to limit the cross-modulation performance of the overall amplifier, and after investigations into the tuning and tracking problems peculiar to the use of voltage variable capacitors for RF tuning elements, the next phase of the development involved the design consideration of the RF amplifier per se. This investigation began by measuring pertinent parameters of many transistor types. A device was sought which had good low noise performance with reasonable gain. The 2N2363 was selected and the rest of the RF amplifier was designed around its characteristics.

4.1.3.1 The Double Tuned Circuit (Report No. 3)

From considerations of image rejection and cross-modulation performance in the transistor stage, it is desirable to keep the pass-band of the double tuned circuit as narrow as posible. However, a practical limit to the unloaded Q of the coils exists, and when transducer loss and noise

figures are also considered, restrictions must be placed on the unloaded to loaded Q ratio, primary to secondary loaded Q ratio, and coefficient of coupling ratio. A detailed investigation into the double tuned circuit was made including the effects of mismatch ratio, limitation of input Q because of VSWR - mismatch loss, transducer loss, coefficient of coupling loss, variation of transducer loss due to variation in the transistor input impedance, noise figure of the double tuned circuit, and primary voltage as a function of Q. It was shown that the primary Q is determined by the permissible input VSWR and by the coefficient of coupling while the secondary Q is a function of the input Q, coefficient of coupling and desired overall bandwidth. The primary off-tune voltage, of particular importance since crossmodulation due to the VVC's is most severe in the input circuit, was shown to be reduced as the coefficient of coupling was reduced below unity. An increase in insertion loss, and hence, in noise figure resulted but this was of the order of 0.5 db for kQ = 0.7, while crossmodulation performance improved such that 10 db additional undesired signal could be applied to the input for the same crossmodulation as with kQ = 1.

4.1.3.2 Transistor Parameters (Report No. 3)

Measured parameters for a batch of 2N1405 transistors was presented and a discussion of the test circuits and method of measurement was given. The 2N2363 transitor, which is a 2N1405 device in a 4 lead TO-18 case, was chosen for the RF amplifier because of its desirable gain characteristics as well as low noise properties. Furthermore, MIL approval had been applied for.

4.1.3.3 Crossmodulation in the Transistor (Report No. 3)

Results of a theoretical analysis for crossmodulation properties of transistors developed by A. H. J. Nieveen and J. J. Sips of the Phillips Semiconductor Laboratory in Holland were quoted, and measured data on the 2N2363 was presented. It was shown that if a small unbypassed emitter-resistor was used in the RF amplifier circuit, the allowable level of undesired signal on the base of the transistor varied as a function of emitter current. The

above mentioned theoretical analysis showed that a complete cancellation of crossmodulation occurred at a specific emitter current, but the measured data shown in Report No. 3 did not bear this out although a definite peak in the level of undesired signal was noted. An explanation for the discrepancy is given now.

It was noted that if the level of undesired signal was kept constant and the crossmodulation index was measured, a complete cancellation of crossmodulation distortion did indeed occur at a particular bias current for a given unbypassed emitter resistor. If the level of the undesired signal was changed, however, the dip occurred at a different emitter current. Now the data presented in Report No. 3 was taken for a fixed crossmodulation index, specifically -20 db crossmodulatio and when the emitter current was changed, the undesired signal was varied until -20 db crossmodulation occurred. Therefore, the position of the dip varied with the undesired signal level as well as the emitter current. The above mentioned analysis neglected the influence of second order curvature in the base emitter diode of the transistor, and it is believed that if account is taken of this, the theory can be extended to accurately predict the results obtained in Report No. 3. A theoretical analysis is presently under way and a complete discussion will be given in the next report. Figures 1 and 2 illustrate the discussion presented above.

4.1.3.4 Conclusion Concerning Transistor Crossmodulation

Calculations based on a double tuned circuit with a loaded Q = 80 showed that an interfering signal of 10V amplitude displaced 8 per cent from the central frequency of the tuned circuit would result in a signal of 13.7 mv on the base of the transistor. Using a 10 ohm resistor in the emitter circuit of the RF amplifier and an emitter current of 2 ma, the allowable signal for -20 db crossmodulation was measured at about 65 mv. Therefore, it can be safely assumed that crossmodulation due to the transistor is negligible in this application.

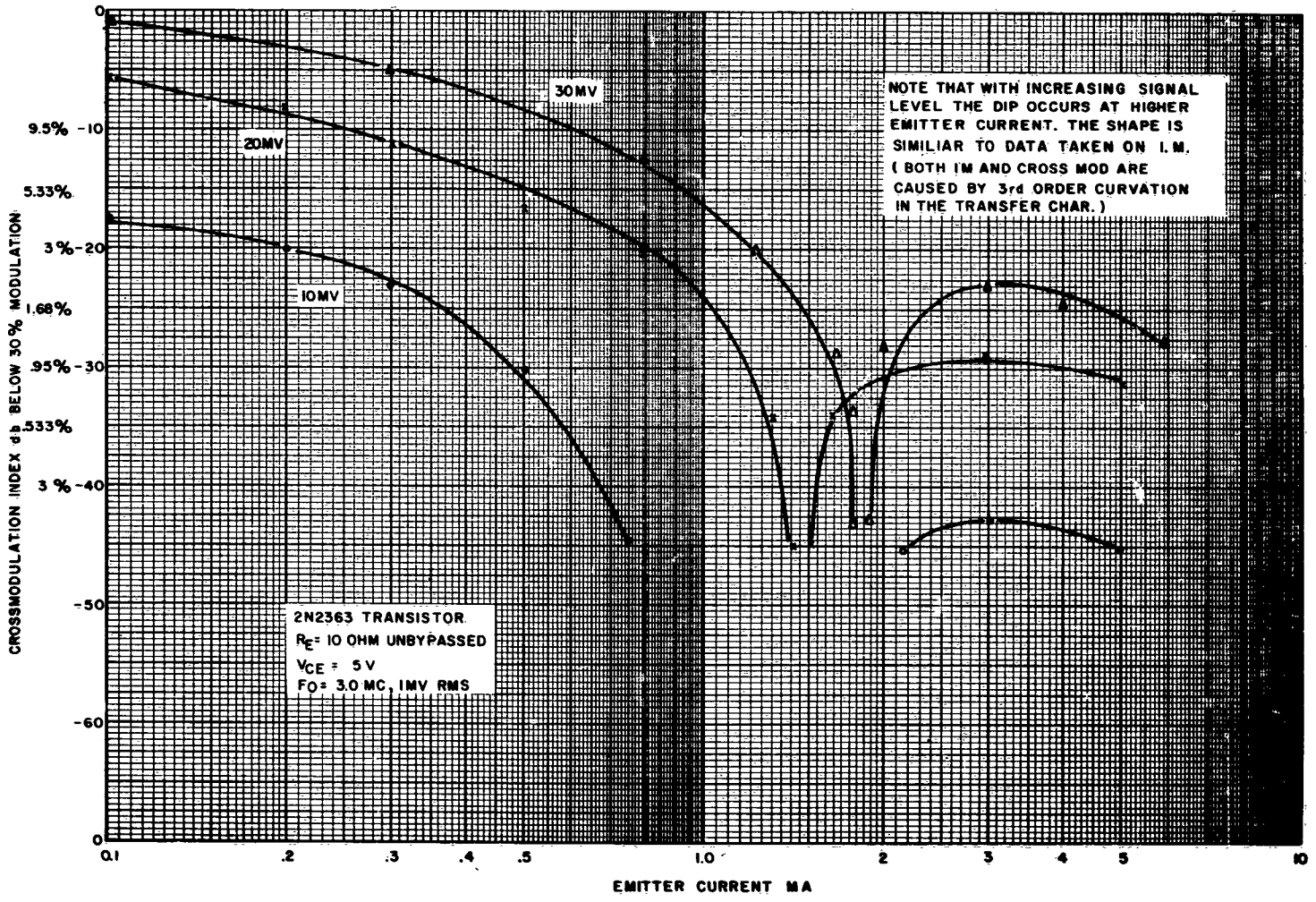

Figure 1. Variation in Cancellation of Crossmodulation as Undesired Signal Amplitude is Varied.

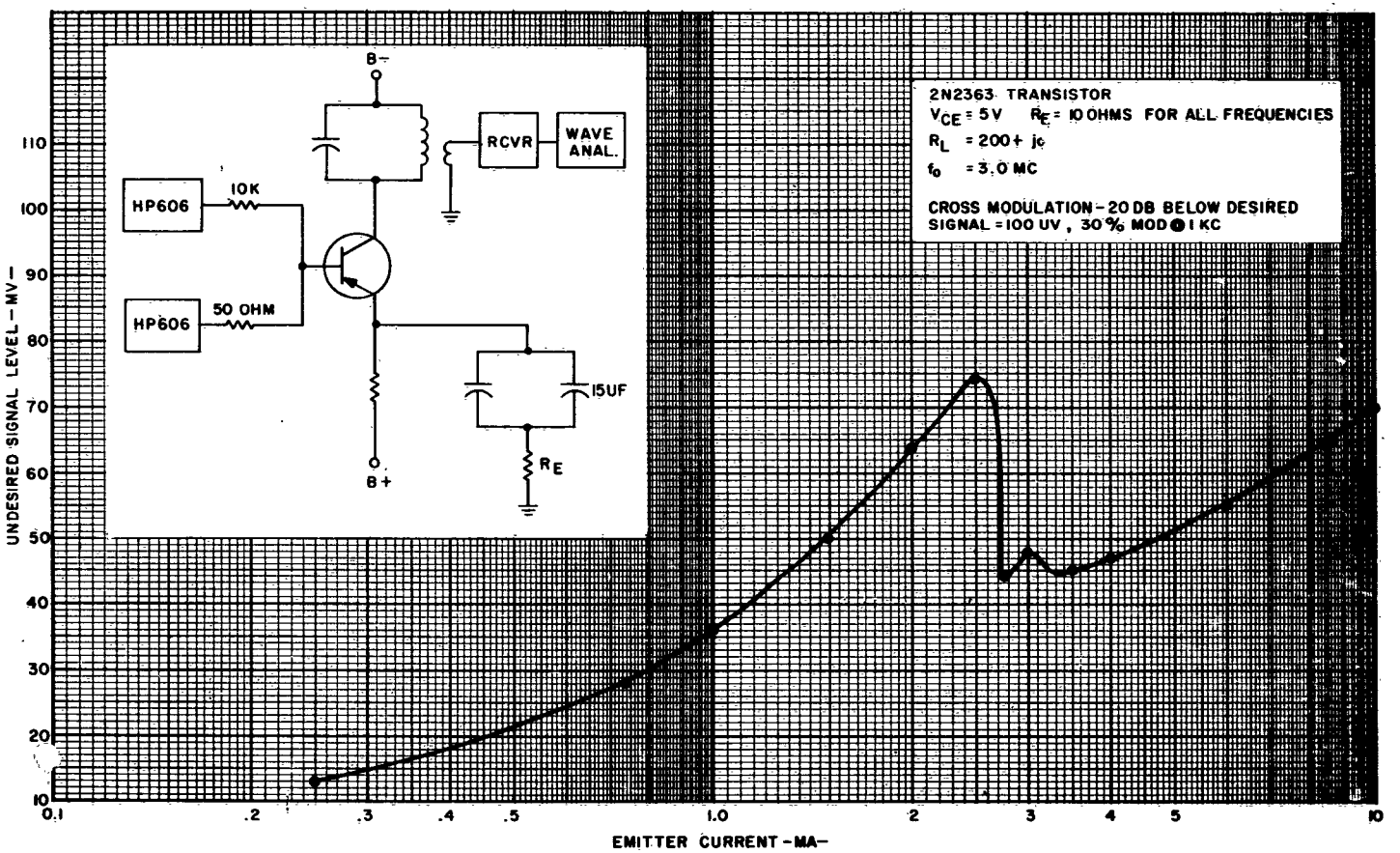

Figure 2. Undesired Signal Level vs. Emitter Current For -20 db Crossmodulation.

4.1.3.5 Degradation of Noise Figure Due to Unbypassed Emitter Resistors

It was expected that the noise figure of the transistor would be degraded as the amount of unbypassed emitter resistance was increased, but the magnitude of the degradation was not known. Experiments were run on some 2N2363 transistors measuring noise figure for various unbypassed emitter resistors as a function of source resistance with emitter current as a parameter. The results are shown in Figures 3. As can be seen, for small resistances, the degradation in minimum noise figure is not appreciable but the optimum source resistance changes.

4.1.3.6 Intermodulation Distortion and AGC (Report No. 4)

When it was established that in order to obtain good crossmodulation performance in the transistor amplifier, a fixed emitter current would be necessary, the problem of AGC took on a new significance. Use of any scheme which varied the emitter current was undesirable and recourse to electronic attenuators was necessary. The amount of AGC required was to a large extent determined by the signal handling capability of the transistor stage. Data taken on a test circuit with various transistor types indicated that the allowable signal level on the base of a common emitter amplifier stage for a given amount of intermodulation distortion was virtually independent of everything including source and load impedance, transistor type, collector to emitter voltage, and emitter current. It should be noted at this point that the emitter circuit contained no unbypassed emitter resistance. Subsequent investigations showed that substantial improvement in IM could be realized by using a small unbypassed emitter resistor and adjusting the emitter current. A theoretical analysis under preparation shows that IM is caused by 3rd order curvature in the transfer characteristic of an amplifier, as is crossmodulation. Hence, if crossmodulation goes through a minimum so too does intermodulation distortion. Figure 4 shows typical data for a 2N2363 amplifier stage with a 10 ohm emitter resistor.

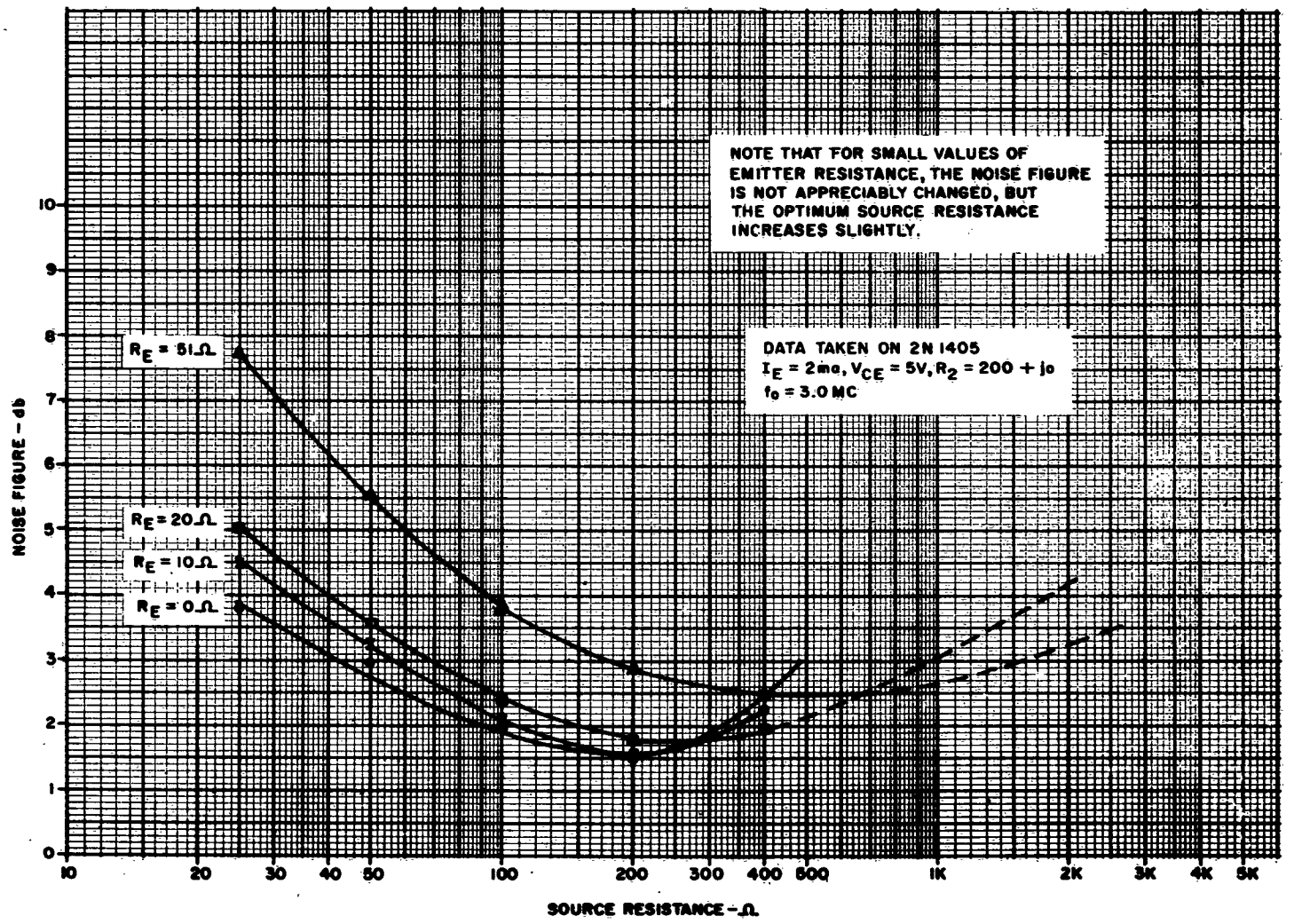

Figure 3. Noise Figure vs. Source Resistance With Unbypassed Emitter Resistance as a Parameter.

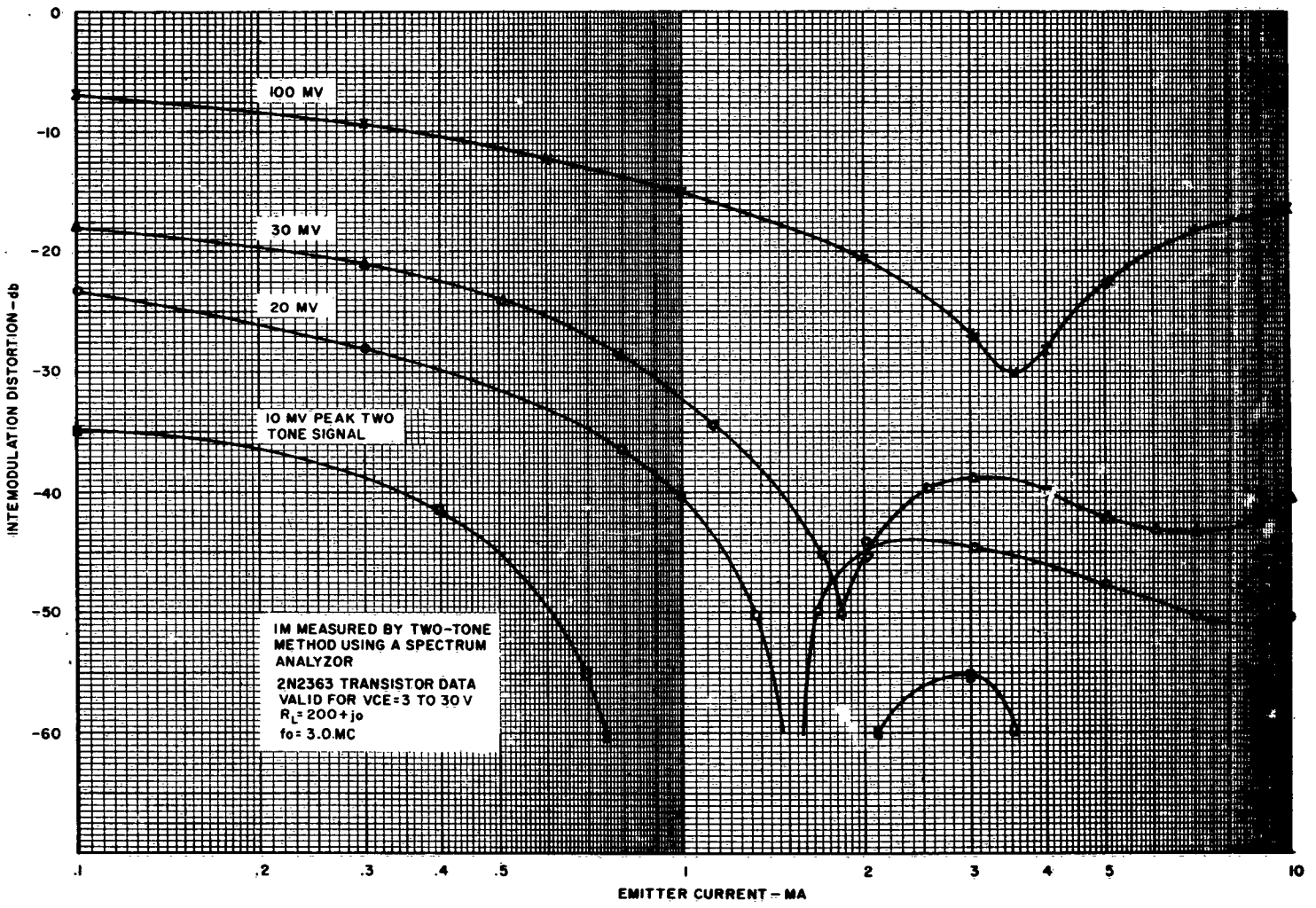

Figure 4. Intermodulation vs. Emitter Current.

4.1.3.7 Electronic Attenuators for AGC (Report No. 4)

A number of electronic attenuator circuits were investigated with the intent of finding a configuration which would provide sufficient control and yet contribute negligible distortion itself. Among the circuits discussed were negative feedback AGC obtained by using a diode in series with the emitter bypass capacitor. When the diode was forward biased, the capacitors were effectively shorted to ground and the amplifier gain was maximum. As the diode current was lowered, however, the impedance increased and the bypass became less effective resulting in a decrease in amplifier gain. Up to 25 db control per stage could be realized with this circuit with currents of 0 to 15 ma. Using shunt diode attenuators in the base circuit of the transistor stages and the negative feedback circuit approximately 50 db AGC control was realizable while series diode arrangements brought the range up to 65 db. The series diode arrangement required only 0 to 2 ma. control current. Attenuators ahead of the double tuned circuits were not usable because they generated crossmodulation.

A number of experiments were run using tungsten filament lamps as the variable resistance element. Primary disadvantages were limited control range (≈10 db) high current (up to 20 ma.) and susceptibility to desensitization when used ahead of the double tuned circuit. The lamp did not cause crossmodulation, however.

4.1.3.8 Bandswitching

Investigations were conducted to determine the feasibility of electronic bandswitching of the tuned circuits. A variety of diodes were measured for RF impedance versus current for various frequencies. In general, the diodes were found to have too high a series RF impedance so that when used to switch the coils across the VVC's the circuit Q was degraded too severely. Figure 5 contains a list of some of the diodes tried and shows results of the measurements. Circuit loaded Q degradation varied from 25 per cent to 60 per cent depending on diode. Even a degradation of 25 per cent was considered too high so consideration was given to a mechanically switched wafer.

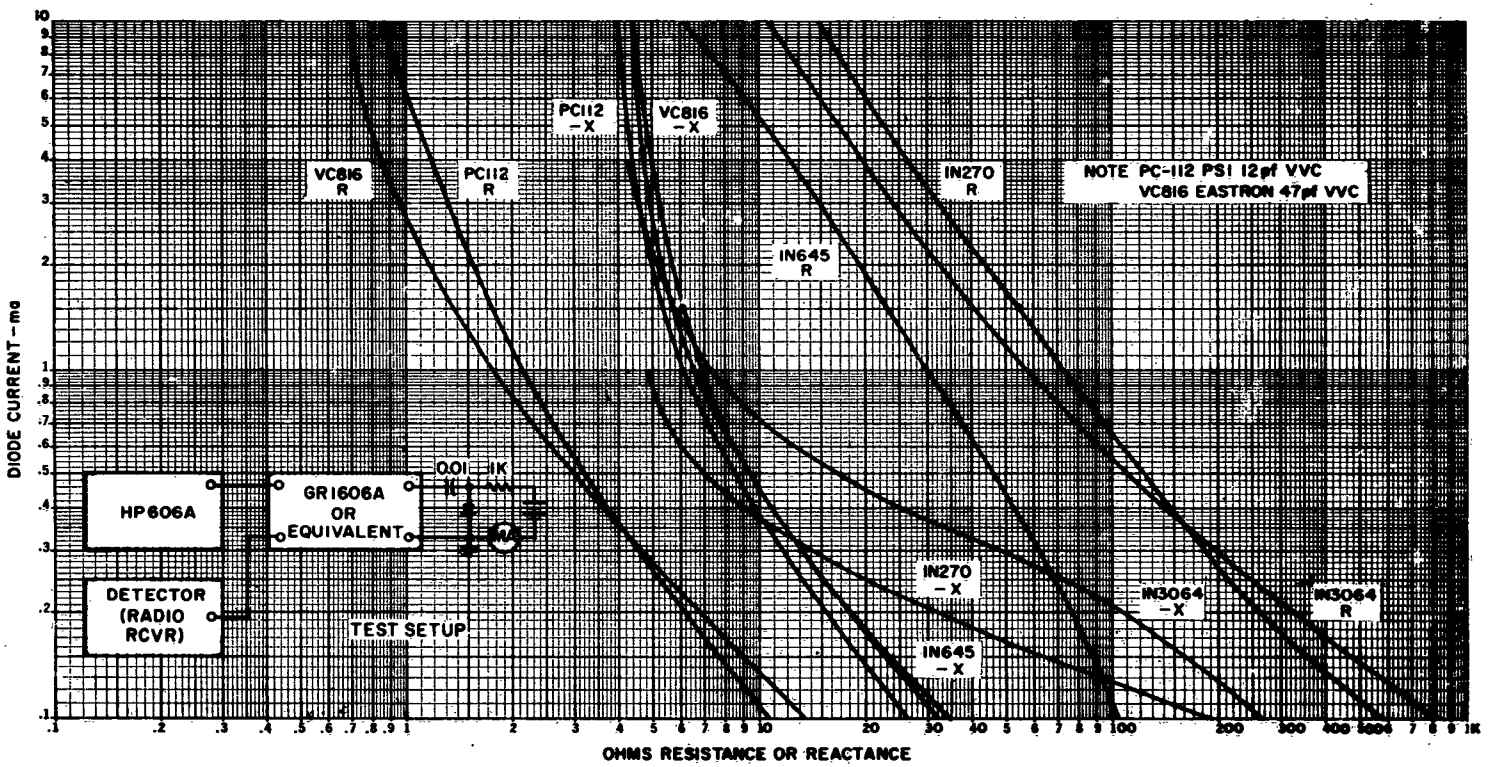

Figure 5. Series RF Impedance of Some Semiconductor Diodes and Voltage Variable Capacitors.

4.1.3.9 The Preliminary Model (Report No. 4)

A preliminary model of the tuners comprising Band 1 (3-4 mc) and Band 5 (9-12 mc) was built using the results of experiments described to this point. Measurements of noise figure and crossmodulation were published in Report No. 4 as well as a complete schematic.

4.1.4 Design of the Digital Tuning Scheme (Report No. 5)

Report No. 5 discussed generation of the coarse digital tuning voltage and described a number of methods for obtaining such a voltage. Advantages and disadvantages of the various methods were pointed out as well as variations on the basic circuits. The method chosen for the Development Models was the last one described, i.e., the Linear Staircase Generator, Diode Shaper, and Output Amplifier Method.

The principle of operation is this: An operational amplifier is set up, such that, the resistors in its input and feedback paths are switched by the digital frequency selection switches so that as frequency is increased in digital steps, the DC output from the operational amplifier increases in discrete voltage increments. (If a high gain amplifier is used in an operational amplifier arrangement, the gain can be shown to be approximately given by $A = -R_f/R_i$ where, R_f is the feedback resistor and R_i is the input resistor). If the weighting of the input and feedback resistors is in a binary coded decimal fashion such as an 8-4-2-1 weighting, four resistors can be used to obtain a decade of gain change in unit increments. Additional decades require four more resistors weighted 80-40-20-10 or .8-.4-.2-.1 depending on whether the gain is a decade lower or higher respectively.

The output from the Linear Staircase Generator is direct coupled to a Diode Shaping Circuit. This circuit which is really a non-linear attenuator, attenuates or "shapes" the linear input so that it fits on the non-linear voltage versus frequency curve which defines the VVC tuning. A DC voltage amplifier amplifies the shaper output to the final required voltage level.

The Linear Staircase Generator output is a DC voltage between the limits of 0 and +20 VDC depending on the frequency selected by the digital frequency knobs. The Diode Shaper output is DC between the limits +20 and +16.5 VDC depending on input, and the final Output Voltage Amplifier is DC between the limits 0 and -61 VDC, corresponding to the coarse digital tuning voltage required to tune the VVC's to the frequency selected.

Figures 6 and 7 are the schematics of the Linear Staircase Generator and Diode Shaper, and the Output Voltage Amplifier respectively.

Design of these amplifiers was aimed at obtaining high open loop gain with an absolute minimum of current. To this end, the 2N930 transistor was selected. The guaranteed minimum β of this transitor is 100 at 5 μa. Maximum advantage of this high β was taken in the design of these amplifiers. Open loop gain greater than 4000 was designed for; the current required for operation of these amplifiers as shown in Figure 7.

4.1.5 Design of the DC - DC Converter - General

The Digital Coarse Tuning Circuitry required three regulated voltages in order to obtain the stability required to remain within the pull-in range of the phase-locked loop with variations in input voltage. (The Digital Coarse Tuning Voltage tunes the signal and oscillator circuits to within the pull-in range of the phase-locked loop which then provides a fine correction and precisely tunes the RF circuits on frequency. See paragraph 4.1.2.3 of this report.) Measurements indicated that the Differential DC Amplifier in the phase-locked loop was also quite sensitive to variations in B+. To accommodate these circuits, a regulated DC-DC converter was designed. (Refer to Figures 8a and 8b.)

4.1.5.1 Design Requirements

The primary consideration was to obtain the highest efficiency consistent with adequate performance from the converter. The input voltage source was assumed to be a lead-acid storage battery nominal 27 VDC system with limits of 20 to 32 VDC. Three different regulated outputs were

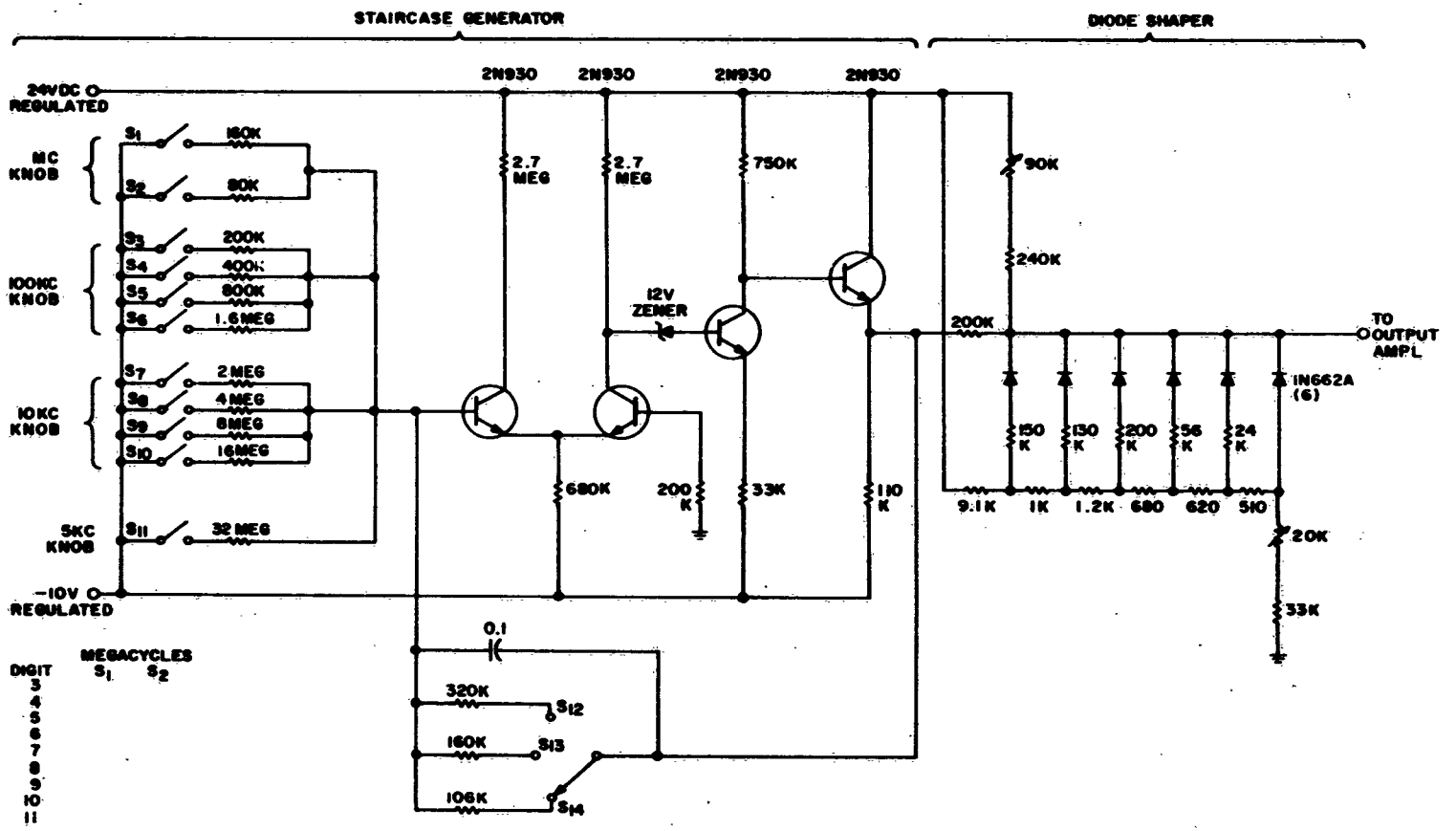

Figure 6. Precision Integrated Tuner Staircase Generator and Diode Shaper Circuit

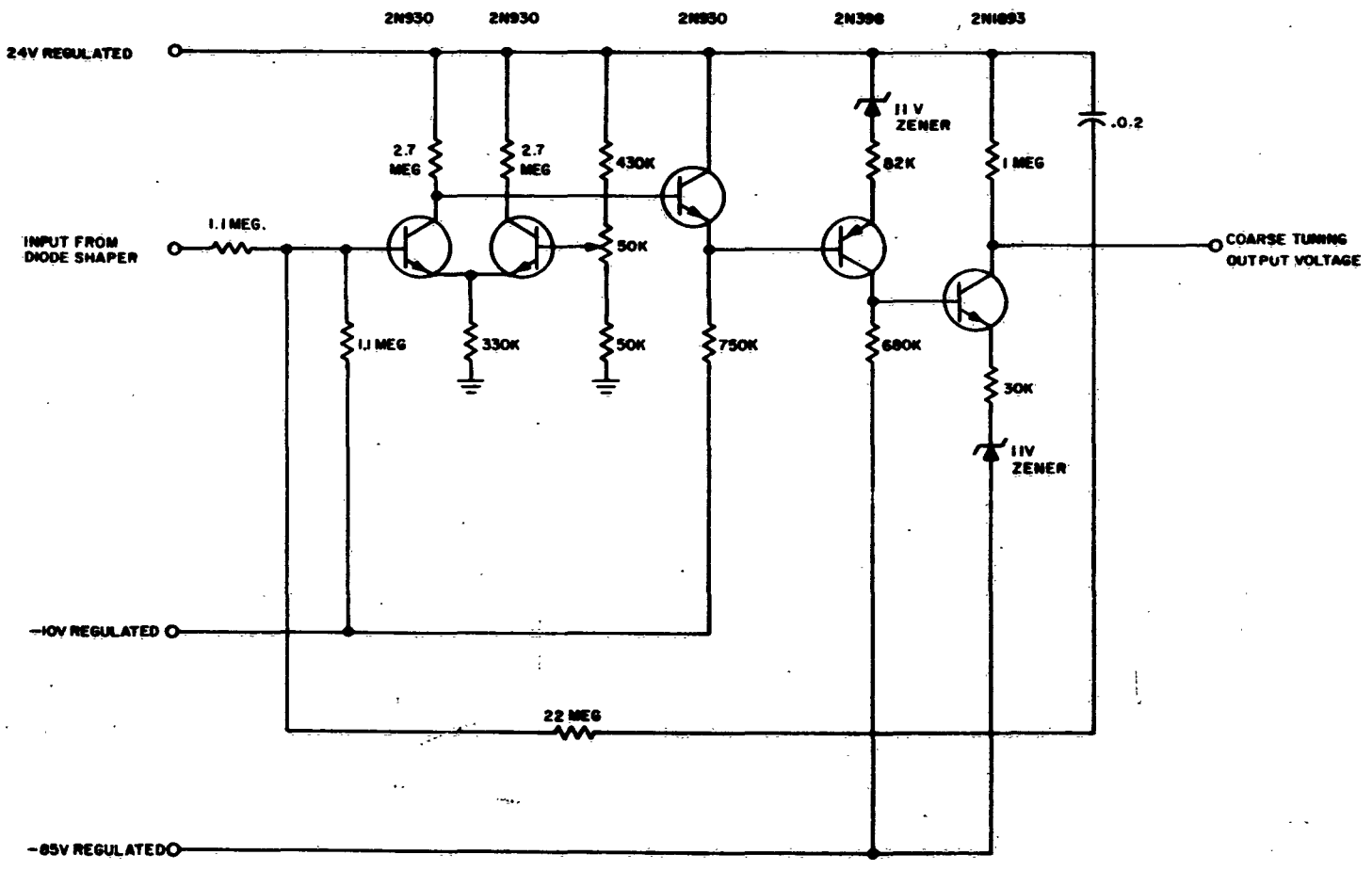

Figure 7. Precision Integrated Tuner Coarse Tuning Output Voltage Amplifier

	BAND END	+24 V REG.	-10 V REG.	-85 V REG.	24 UNREG. EQUIV. INPUT (ASSUMES 100% CONVERSION EFFICIENCY)
Staircase Generator	Low Freq.	.05 ma	.160 ma		
	High Freq.	.44 ma	.458 ma		
Diode Shaper	Low	.487 ma			
	High	.55 ma			
Output Amplifier	Low	.175 ma	.031 ma	.04 ma	
	High	.46 ma	.048 ma	.128 ma	
Total of Above CKTS	Low	.725 ma	.18 ma	.04 ma	.941 ma
	High	1.1 ma	.39 ma	.128 ma	1.72 ma
Total Input Power	Low	17.4 mw	1.8 mw	3.4 mw	22.6 mw
	High	26.4 mw	3.9 mw	10.9 mw	41.2 mw

Figure 8a. Input Current Requirements For The Digital Coarse Tuning Circuits

	INPUT WITHOUT REGULATOR	INPUT WITH REGULATOR
No Load Convertor Input	2.3 ma @ 17 VDC	2.4 ma @ 18 to 32 VDC
Full Load Convertor Input *	17 ma @ 17 VDC	17 ma @ 18 to 32 VDC
Efficiency, Full Load	86%	89% @ 24 VDC Input

*Includes 9 ma @ +24 VDC Reg. Required For Phase Locked Loop Circuitry

Figure 8b. Input Requirements To The DC-DC Convertor

required, and to use three series pass elements not only would have been inefficient in terms of power required, but would have required a large number of components with attendant increases in size. Examination of the load requirements and the changes in load requirements over the operating range of the equipment indicated that input regulation might be adequate. Figure 9 shows the schematic and block diagram of the DC-DC Converter which was designed. Use of a feedback winding on the square loop core transformer to control the output regulation depends on the tightness of the coefficient of coupling between the various windings and for toroids this is characteristically near unity. A problem occurs, however, when one of the outputs has a large load variation, because its reflected impedance causes a feedback correction which tends to minimize the error caused on that particular winding but introduces an error in those windings that do not have a simultaneous load variation. At best then, only an approximate correction for load variations can be had, if more than one load winding is required on a transformer. Fortunately for this application, load changes on all the windings tend to be in the same direction, i.e., they increase together (although not by the same percentage). Regulation with input voltage variation is excellent, and because the load variations are not too large, the overall regulation is quite good. This is given in Figure 10. Efficiency, input current requirements and so on for this design are given in Table II. It is felt that a refined design can improve the overall efficiency of the converter, and if a smaller variation in unregulated input voltage can be assured, far less power would be dissipated in the regulator. Such would be the case with a nickel cadmium or mercury cell battery for example.

4.1.6 The Development Models

4.1.6.1 Constraints on Packaging

Miniaturization efforts were restricted by a combination of fundamental component limitations. Crossmodulation distortion limited the available tuning range of the voltage variable capacitors by limiting the minimum bias voltage. This plus allowable circuit stray capacitance determined the number of bands required to cover 3 to 12 mc, and therefore, the number of coils needed.

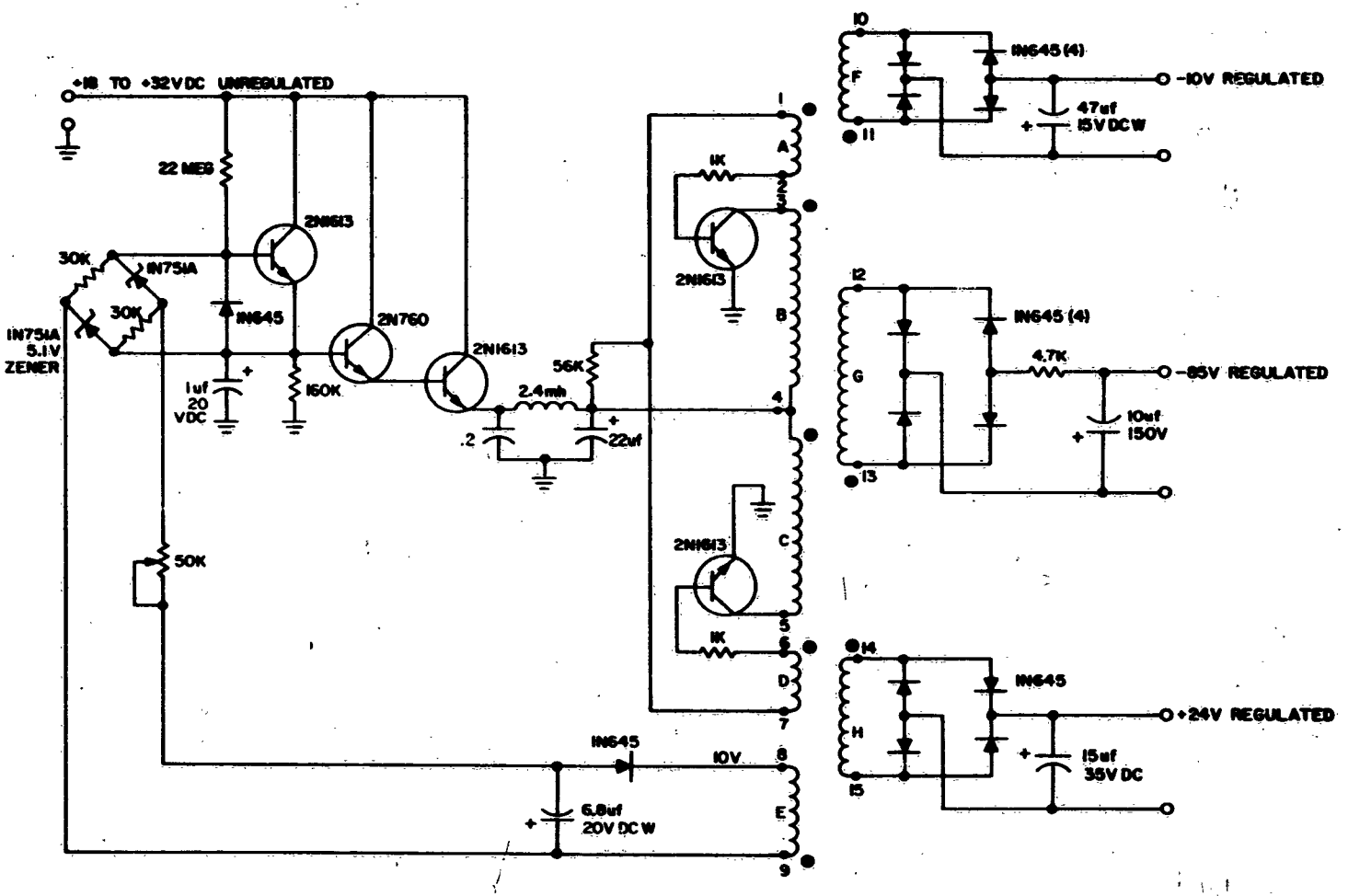

Figure 9. Precision Integrated Tuner DC-DC Converter, Schematic

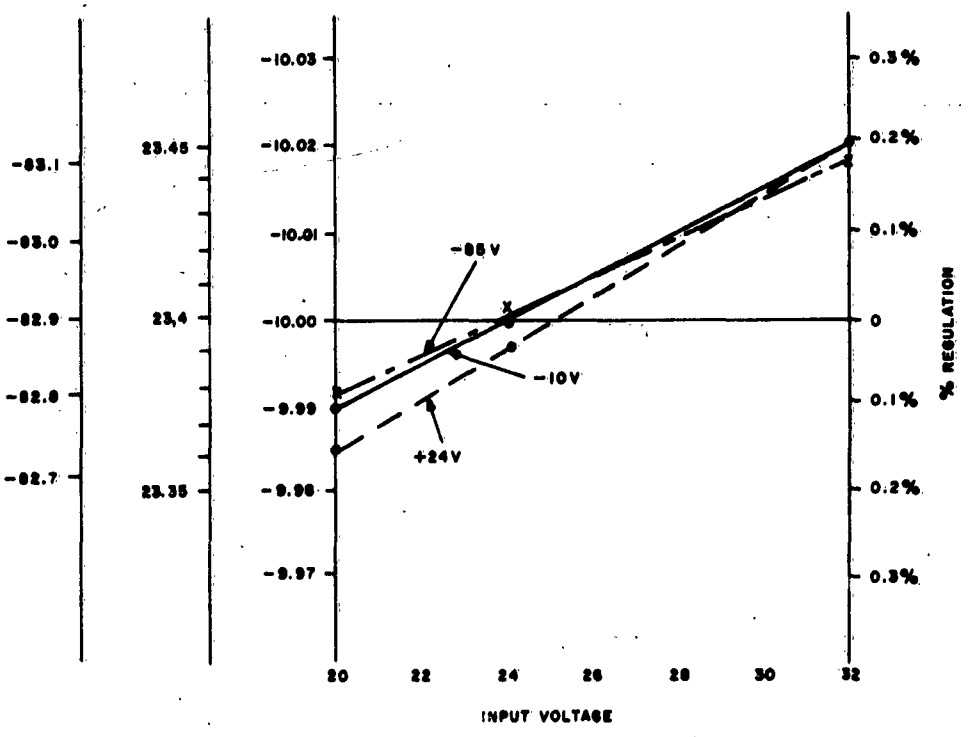

Figure 10. Full Load Regulation vs. Input Voltage Variations

The temperature specification predicated the use of powdered iron coils, but these have a large physical size. With an emphasis on obtaining the smallest possible volume it was decided that the higher permeability ferrite cores should be used, since the coil size would be much smaller. Although the then available ferrites had rather poor temperature characteristics, information obtained indicated that a number of low temperature coefficient high frequency materials were under development and future designs could incorporate these materials.

4.1.6.2 The Tuner

It was recognized early that the tuner could not be packaged in a volume less than about 8 cubic inches. Of all the possible band switching techniques considered, a rotating turret containing the RF coils was deemed most practical. The RF amplifiers and tuned circuits were packaged in modules which fitted around the turret, and the wafers on which the coils were mounted provided the needed switch contacts.

Figure 11 is a photograph of the present tuner design. Complete electrical performance data on this design is not available at the time of this writing but will be presented in the next report.

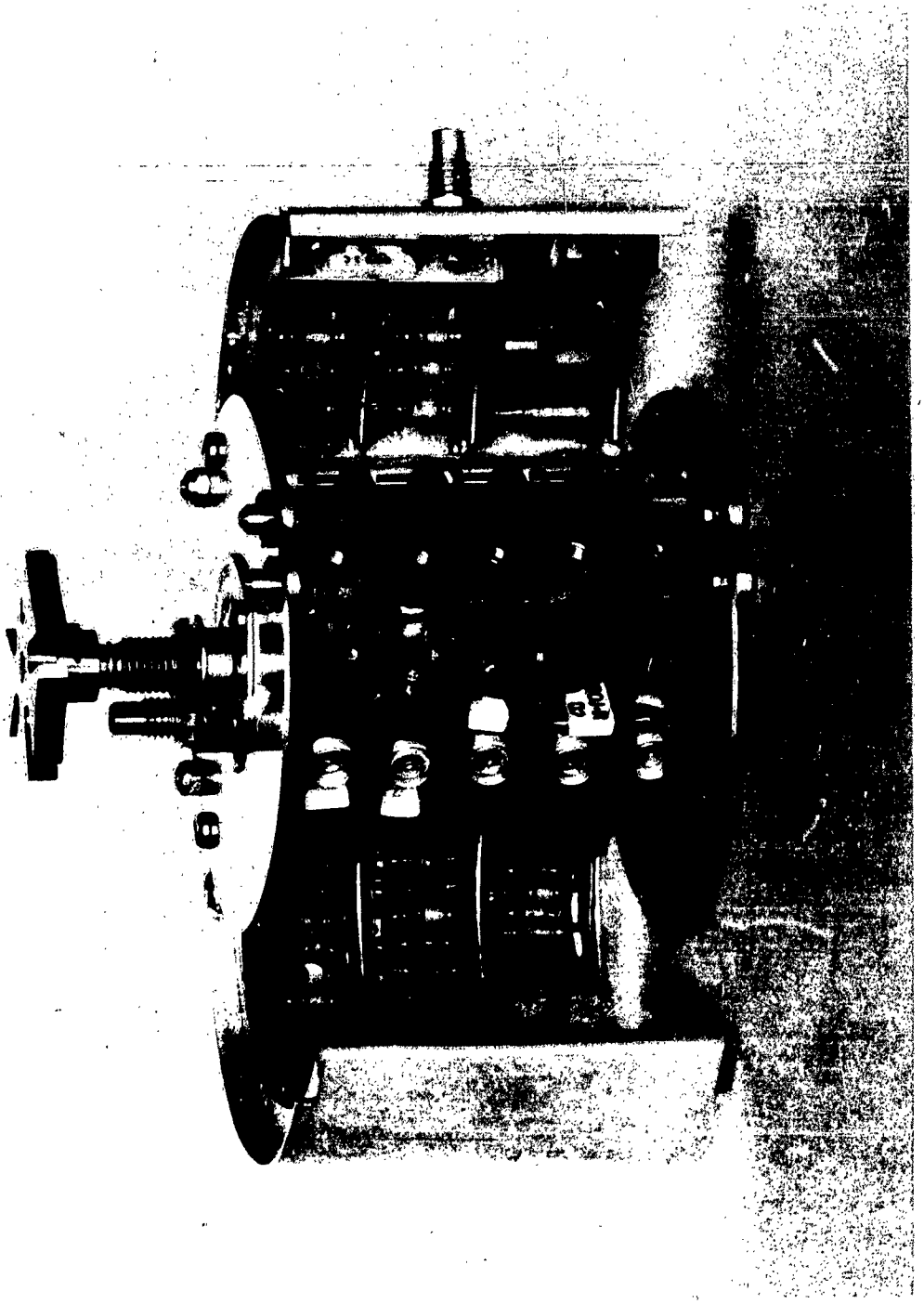

Figure 11. Integrated Precision Tuner, Present Design

4.2 VOLTAGE VARIABLE CAPACITOR REQUIRED FOR OCTAVE TUNING

The relationship between frequency and capacitance can be expressed as:

$$\left(\frac{f_2}{f_1}\right)^2 = \frac{C_1'}{C_2'} = \frac{C_1 + C_{ST}}{C_2 + C_{ST}}$$

For 2:1 frequency ratio, $(f_2/f_1) = 2$ and $(C_1'/C_2') = 4$

$$\frac{C_1 + C_{ST}}{C_2 + C_{ST}} = 4$$

$$C_1 + C_{ST} = 4(C_2 + C_{ST}) = 4C_2 + 4C_{ST}$$

$$C_1 = 4C_2 + 3C_{ST}$$

for $C_1 = 5C_2$, $C_2 = 3C_{ST}$

for $C_1 = 4.5C_2$, $C_2 = 6C_{ST}$

Breaking this down into the actual values required for various strays:

C_{ST}	$C_1/C_2 = 5$	$= 4.5$
5	75/15	135/30
10	150/30	270/60
15	225/45	405/90
20	300/60	540/120
25	375/75	675/150
30	450/90	810/180

A reasonable assumption for C_{ST} is 10 to 15 pf for the high packaging density expected. This will eliminate a capacitance ratio of 4.5 to 1 because a maximum capacity of 300 to 450 pf would be required but if the Philco unit can be extended in voltage breakdown, it would be quite usable. To determine the maximum and minimum voltages required to obtain the required capacitance ratio:

$$C = KV^{-x}$$

$$\log\frac{C_1}{C_2} = x\log\frac{V_2'}{V_1'} = x\log\frac{V_2 - 0.5}{V_1 - 0.5}$$

$$\log\frac{V_2 - 0.5}{V_1 - 0.5} = \frac{\log\frac{C_1}{C_2}}{x}$$

The exponent has been measured for several capacitors, as shown in Figure 12.

For $C_1/C_2 = 5$:

$x = 0.44$ (Philco)

$$\log\frac{V_2'}{V_1'} = \frac{.699}{0.44} = 1.583$$

$$\frac{V_2'}{V_1'} = 38.3$$

$$V_2 = 38.3(V_1 - 0.5) + 0.5$$

$$= 38.3\,V_1 - 18.7$$

For $C_1/C_2 = 4.5$:

$$\log\frac{V_2'}{V_1'} = \frac{.653}{0.44} = 1.485$$

$$\frac{V_2'}{V_1'} = 30.5$$

$$V_2 = 30.5(V_1 - 0.5) + 0.5$$

$$= 30.5V_1 - 14.75$$

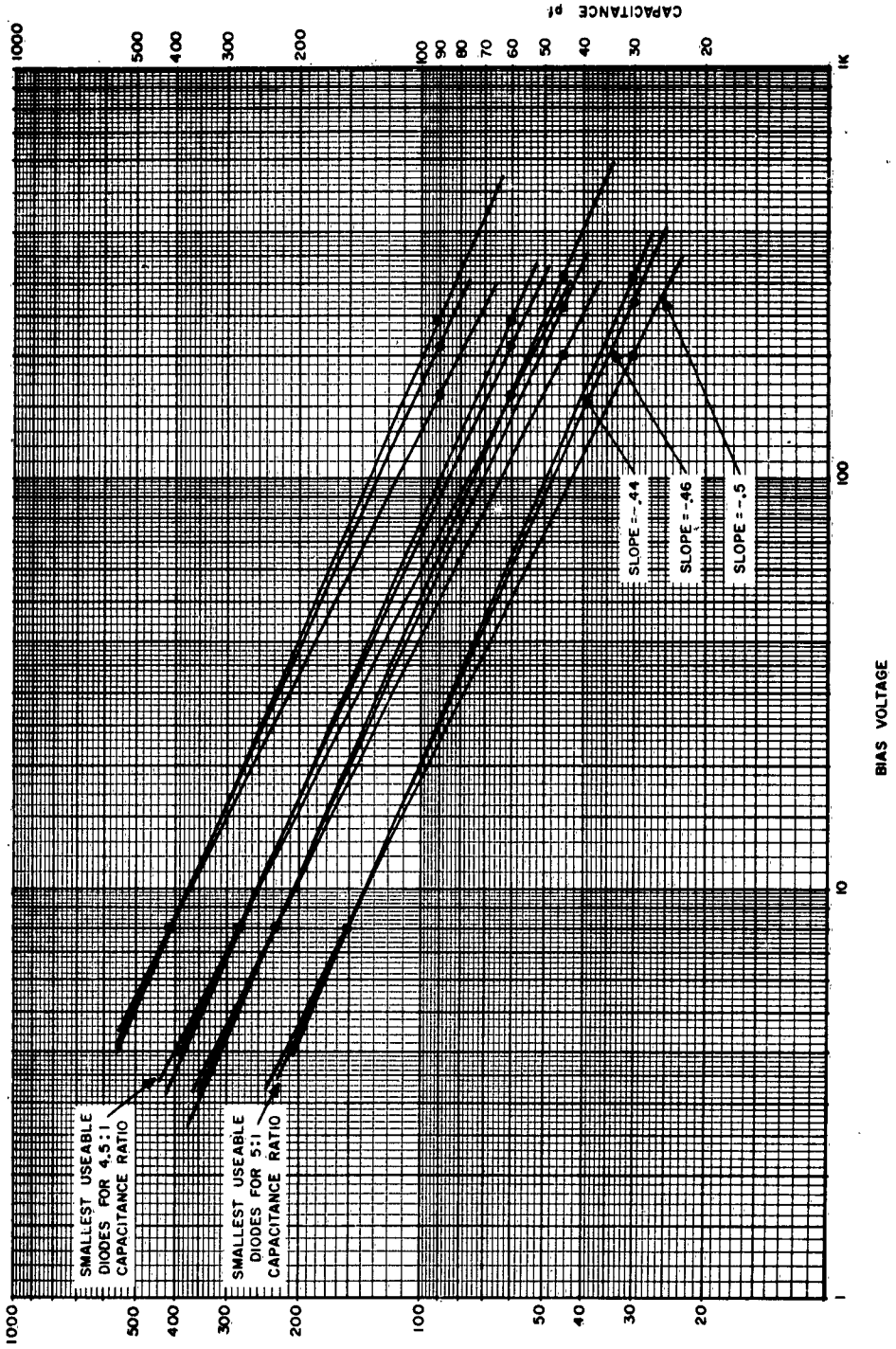

Figure 12. Variation of Capacitance vs. Voltage For General Voltage Variable Capacitors

x = 0.46 (PSI)

$$\log \frac{V_2'}{V_1'} = \frac{.699}{0.46} = 1.52$$

$$\frac{V_2'}{V_1'} = 33.1$$

$$V_2 = 33.1(V_1 - 0.5) + 0.5$$

$$= 33.1V_1 - 16.1$$

$$\log \frac{V_2'}{V_1'} = \frac{.653}{0.46} = 1.42$$

$$\frac{V_2'}{V_1'} = 26.3$$

$$V_2 = 26.3(V_1 - 0.5) + 0.5$$

$$= 26.3V_1 - 12.6$$

x = 0.5 (Theoretical for Abrupt Junction)

$$\log \frac{V_2'}{V_1'} = \frac{.699}{.5} = 1.397$$

$$\frac{V_2'}{V_1'} = 25$$

$$V_2 = 25(V_1 - 0.5) + 0.5$$

$$= 25V_1 - 12$$

$$\log \frac{V_2'}{V_1'} = \frac{.653}{.5} = 1.305$$

$$\frac{V_2'}{V_1'} = 20.2$$

$$V_2 = 20.2(V_1 - 0.5) + 0.5$$

$$= 20.2V_1 - 9.4$$

We know that, at bias voltages less than 8 volts, cross-modulation becomes excessive. While this is a function of the capacitor non-linearity as well as tuned circuit parameters, assume that this is the minimum voltage we can tolerate, at least until it can be reasonably confirmed otherwise by experiment or theory.

Then possible capacitors for the conditions $V_{BIAS} = 8V$ min

$C_1\Big|_{8V}$ = 150, 225, 270, and 405 pf.

For a reverse biased diode, V_1 is negative.

$$\therefore \quad x = .44 \quad V_2 = 38.3V_1 - 18.7 = -306$$
$$x = .46 \quad V_2 = 33.1V_1 - 16.1 = -265$$
$$x = .50 \quad V_2 = 25V_1 - 12 = -200$$

for $C_1/C_2 = 5$, $C_2 = 30$, 45 pf; $V_1 = 8V$

$$x = .44 \quad V_2 = 30.5V_1 - 14.75 = -244$$
$$x = .46 \quad V_2 = 26.3V_1 - 12.6 = -210$$
$$x = .50 \quad V_2 = 20.2V_1 - 9.4 = -162$$

for $C_1/C_2 = 4.5$, $C_2 = 60$, 90 pf; $V_1 = 8V$

It is to our advantage to use the largest capacitance with the highest possible exponent, at least from the ease of tuning standpoint.

An estimate of Junction Area can be made from the equation below:

$$C_j = \left(\frac{\epsilon}{2\mu\rho}\right)^{1/2} V_B^{-1/2}$$

$\epsilon = 11.7 \times 8.854 \times 10^{-4}$ farad/cm $= 1.035 \times 10^{-12}$ for silicon

$\mu = 1200$

$\rho = 10\Omega$ cm (assumed)

$$C_j = \left[\frac{1.035 \times 10^{-12}}{2(1200)}\right]^{1/2} (\rho V_B)^{-1/2} = (4.32 \times 10^{-16})^{1/2} (\rho V_B)^{-1/2}$$
$$= 2.08 \times 10^{-8} (\rho V_B)^{-1/2} = 2.08 \times 10^{4} (\rho V_B)^{-1/2} \text{ pf/cm}^2$$

assuming $\rho = 10\Omega$ cm, $V_B = -8V$

$$C_j = .233 \times 10^{4} \ \mu\mu\text{f/cm}^2 = 2330 \ \mu\mu\text{f/cm}^2$$

$$A_{150\ pf} = \frac{150}{2330} = .0641\ cm^2$$

$$.0641\ cm^2 \left(\frac{1\ in}{2.54\ cm}\right)^2 \cong .01\ in^2$$

$$A_{225\ pf} = (.01)\ \frac{225}{150} = .015\ in^2$$

$$A_{270\ pf} = .018\ in^2$$

$$A_{405\ pf} = 0.27\ in^2$$

$$A_{60\ pf} = .004\ in^2$$

Since the probability of obtaining an imperfection free area goes up as the area goes down, economics should determine an optimum capacitor size, balancing the ease of junction fabrication to the number of diodes required in the equipment for the final desired C.

4.2.1 CALCULATION OF THE QUANTITY OF 1N3557 DIODES REQUIRED TO TUNE THE 3 to 12 mc RANGE IN THREE BANDS

A capacitance ratio of 4.6:1 is obtained by biasing the 1N3557 over the limits of 8 to 200 volts.

Assuming 15 pf stray and three bands 3 to 5 mc, 5 to 8 mc, and 8 to 12 mc:

$$\frac{C_1 + C_{ST}}{C_2 + C_{ST}} = 1.665^2 = 2.78 \qquad \text{i.e. 3:5 mc in first band}$$

$$C_1 + C_{ST} = 2.78\,C_2 + 2.78\,C_{ST}$$

$$C_1 = 2.78\,C_2 + 1.78\,C_{ST}$$

for $C_1 = 4.6\,C_2$

$$4.6\,C_2 = 2.78\,C_2 + 1.78\,C_{ST}$$

$$1.82\,C_2 = 1.78\,C_{ST}$$

$$C_2 = 0.98\,C_{ST} \approx C_{ST} = 15 \text{ pf}$$

The 1N3557 has a nominal capacitance of 23 pf at 8 volts and 5 pf at 200 volts. Three 1N3557 capacitors would be required in a parallel configuration, or six in a series-parallel arrangement.

4.2.2 CALCULATION OF MINIMUM BIAS REQUIRED TO TUNE THE 5 to 7 mc BAND USING THE 1N3557 VARICAP®

Band 3 on the present unit tunes from 5 to 7 mc, a frequency ratio of 1.4:1, a capacitance ratio of 1.82:1. C_{ST} = 12 pf.

$$\frac{C_1 + 12}{C_2 + 12} = 1.82$$

$$C_1 + 12 = 1.82C_2 + 21.84$$

$$C_1 = 1.82C_2 + 9.84$$

At 200 volts, $C_2 = \frac{5 \text{ pf}}{\text{diode}} \times 3 \text{ diodes} = 15 \text{ pf}$

$$C_1 = (1.82)(15) + 9.9 = 27.3 + 9.9 = 37.2 \text{ pf or } 12.4 \text{ pf/diode}$$

This occurs at a bias voltage of about 30 volts.

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5. CONCLUSIONS

A review of the complete design of the tuner has been given here. Summaries of all the design considerations and the constraints which lead to the present Development Models have been presented. While the specification objectives have not been completely satisfied, enough work has been completed to indicate that a tuner can be made which will meet all the electrical specification requirements provided that a more suitable voltage variable capacitor becomes available. Considerations leading to a specification for such a diode are included in paragraph 4.2 of this report.

To summarize then, the program to date has shown that:

1. Neglecting crossmodulation caused by the VVC's, a transistorized RF amplifier can be designed to cover the 3 to 12 mc frequency range and yield crossmodulation, intermodulation, and sensitivity characteristics comparable to that of the highest performance vacuum tube communications receivers.
2. Extension of the frequency range to 2 to 30 mc does not present a problem insofar as presently available components are concerned.
3. With an improved VVC, octave tuning with improved crossmodulation can be expected. Such a device is theoretically possible and has been made in the laboratory by Philco Corporation. More work is needed in this area in order to obtain a reproducible low cost unit.
4. Electronic tuning of an RF amplifier using VVC's is practical and offers advantages in reduction of equipment size and complexity, particulary where digital tuning is required.

6. PROGRAM FOR NEXT INTERVAL

Work during the next interval will be devoted to two primary objectives. First, measurements on crossmodulation distortion on a variety of new voltage variable capacitors will be made. This data will be aimed at completing the theoretical analysis of crossmodulation in VVC's. Second, data will be accumulated on newly announced silicon RF transistors with low noise figures. It is expected that the germanium device now being used can be replaced with a silicon unit, thereby, obtaining improved high temperature operation of the RF tuner.

7. IDENTIFICATION OF KEY PERSONNEL

The following project personnel spent time in the execution of the work described in this report.

(January 1 to March 31, 1963)

Personnel		Hours
F. S. J. Daniel	Section Head	41
G. J. Luhowy	Project Engineer	542
W. Peck	Technician	737.8
W. Bujalski	Technician	50

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General Dynamics/Electronics, Rochester, New York
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Rept. for:
(SCTR No. SCL-7566A (11 Jan. 61) DA No. 3626-02-001
(Contract No. DA-36-039-SC-88908) Unclassified Report

This report covers the sixth quarter progress in the study of problems associated with electrical tuning of a 3 mc to 12 mc RF tuner. This report is a review of the design and problem areas from the beginning of the program to date. Data on the Digital Coarse Tuning Scheme is presented along with schematics and a description of operation. A discussion of voltage variable capacitor characteristics required to achieve octave tuning is presented.

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